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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,775	07/16/2007	Joerg Gliese	V0195.0093	1128

38881 7590 11/16/2007

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EXAMINER	
TRAN, ANH Q	
ART UNIT	PAPER NUMBER
2819	
MAIL DATE	DELIVERY MODE
11/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,775	GLIESE, JOERG	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-30,43 and 44* is/are rejected.

7)☒ Claim(s) *31-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/4/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 23-30, 43 are rejected under 35 U.S.C. 102(b) as being anticipated by Shiraishi (5,909,386).

Claim 23, Shiraishi shows a logic basic cell (Fig. 1) for forming an output signal (S1) from at least three input signals (Ci, A0 and B0) in accordance with a predeterminable logic function, comprising:

a first logic function block (11, 12, 31 and 32) having two data signal inputs (A0 and B0), to which a first input signal and a second input signal can be applied, and having a data signal output (X) for providing a logic combination of the first input signal and the second input signal in accordance with a predeterminable first logic subfunction;

a second logic function block (21, 22, 41 and 42) having two data signal inputs (A0 and B0), to which the first input signal and the second input signal can be applied, and having a data signal output (X') for providing a logic combination of the first input signal and the second input signal in accordance with a predeterminable second logic subfunction;

a first logic transistor (15) having a first source/drain terminal (X), which is coupled to the data signal output of the first logic function block, having a gate terminal,

at which a third input signal (Ci) can be provided, and having a second source/drain terminal (S1), at which the output signal (Si) can be provided; and

a second logic transistor (25) having a first source/drain terminal (X'), which is coupled to the data signal output of the second logic function block, having a gate terminal, at which a complementary signal (Ci bar) with respect to the third input signal can be provided, and having a second source/drain terminal (S1), which is coupled to the second source/drain terminal of the first logic transistor.

Claim 24, Shiraishi shows the logic basic cell as claimed in claim 23, wherein the first logic function block and the second logic function block in each case have at least one additional data signal input (B1 is connected to transistors 11 and 21), it being possible for an additional input signal to be applied to each of the additional data signal inputs, whereby the logic basic cell is set up for forming an output signal from at least four input signals in accordance with a predeterminable logic function.

Claim 25, Shiraishi shows the logic basic cell as claimed in claim 23, wherein the first logic function block and the second logic function block are each formed from a plurality of data signal transistors (11, 12, 21, 22, 31, 32, 41, and 42 are PMOS and NMOS transistors) that are connected to one another in accordance with the respective logic subfunction.

Claim 26, Shiraishi shows the logic basic cell as claimed in claim 25, wherein:

the logic transistors (15) and the data signal transistors (11, 12, 31, and 32) are transistors of a first conduction type (PMOS transistors, col. 3, lines 55-67) and form a first data signal path, a second data signal path is formed from transistors of a second

conduction type (21, 22, 41, and 42 are NMOS transistors, col. 3, lines 55-67), which is complementary to the first conduction type, in which case, for each of the transistors of the first data signal path, a correspondingly connected transistor is provided in the second data signal path, and the second source/drain terminals of the logic transistors of the first data signal path and the second source/drain terminals of the logic transistors of the second data signal path are coupled to one another (the second source/drain terminals of transistor 15 and 25 are connected to one another at S1).

Claim 27, Shiraishi shows the logic basic cell as claimed in claim 23, further comprising an evaluation switch (52), to which the output signal can be applied, and having a precharge switch (51), which switches are connected and can be controlled such that the output signal (Sn) is provided at an output of the logic basic cell when the evaluation switch is close and the precharge switch is open, and that a reference signal (VDD) is provided at the output of the logic basic cell when the precharge switch is close and the evaluation switch is open.

Claim 28, Shiraishi shows the logic basic cell as claimed in claim 27, wherein each of the evaluation switch and the precharge switch is a transistor (51 and 52 are transistor).

Claim 29, Shiraishi shows the logic basic cell as claimed in claim 23, set up as a CMOS logic (the adder is CMOS logic) basic cell.

Claim 30, Shiraishi shows the logic basic cell as claimed in claim 23, wherein at least one of the logic function blocks is formed as a device selected from the group consisting of a programmable logic device, a field-programmable gate array, a mask-

programmed application specific integrated circuit, a logic gate or arrangement of a plurality of logic gates (OR and AND gates, col. 12, lines 36-57), and a look-up table.

Claim 43, Shiraishi shows the logic basic cell array for forming an arrangement output signal from at least four input signals in accordance with a predeterminable logic function, comprising:

a first logic basic cell as claimed in claim 23;

a third logic transistor (16, Fig. 1) having a first source/drain terminal (Y), to which the output signal of the first logic basic cell can be applied, having a gate terminal, at which a fourth input signal (Ci bar) can be provided, and having a second source/drain terminal (S1), at which the output signal of the logic basic cell array can be provided;

a second logic basic cell as claimed in claim 23; and

a fourth logic transistor (26) having a first source/drain terminal, to which the output signal of the second logic basic cell can be applied, having a gate terminal, at which a complementary signal (Ci) with respect to the fourth input signal can be provided, and having a second source/drain terminal (S1), which is coupled to the second source/drain terminal of the third logic transistor.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiraishi (5,909,386).

Shiraishi discloses the claimed invention except for a plurality of logic basic cell arrays as claimed in claim 43. It would have been an obvious to one having ordinary skill in the art at the time the invention was made to provide an arrays of a plurality of logic basic cell, since it has been held that mere duplication of the essential working parts of a device involved only routine skill in the art.

Allowable Subject Matter

5. Claims 31-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-Th (8:00-6:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANH Q. TRAN
PRIMARY EXAMINER

11/8/07